IN THE SPECIFICATION

Please insert the following paragraph on page 1 after the title of the invention and before the "Technical Field":

--Related Application

This application is a national phase of PCT/JP2004/016938 filed on November 15, 2004, which claims priority from Japanese Application No. 2003-400262 filed on November 28, 2003, the disclosures of which Applications are incorporated by reference herein. The benefit of the filing and priority dates of the International and Japanese Applications is respectfully requested.--

The following paragraphs will replace all prior versions of them in the specification of the application.

1) On page 26, line 22, please amend the following paragraph as follows:

Fig.11 is a an another characteristics chart illustrating effects of the mixer circuit according to the fourth embodiment.

w/ 7.2008 2) On page 38, line 8 23, please amend the following paragraph as follows:

As shown in Fig.6, the mixer circuit according to the third embodiment includes, in addition to that the mixer circuit of the second embodiment of the present invention is provided with the first bypass current source 45 that additionally supplies the bias current only to the RF ~~signal supplier 50~~ transistor 11, further a second bypass current source 46 that is connected between the first IF output terminal 33 and the ground GND thereby to additionally supply a bias current only to the first load resistor 31, and a third bypass current source 47 that is connected between the second IF output terminal 34 and the ground GND thereby to additionally supply a

bias current only to the second load resistor 32. The first to third bypass current sources 45 to 47 are covered by a bypass current supply portion described in Claim 8.

wf 7-20-09 3) On page 43, lines ~~18~~ 1 and ~~21~~ 13, please amend the following paragraph as follows:

The LO signal processing portion 120 includes a first LO transistor 121 which has a source terminal connected to the drain terminal of the first RF transistor 111 and a drain terminal connected to the first IF output terminal 133, a second LO transistor 122 which has a source terminal connected to the drain terminal of the first RF transistor 111 and a drain terminal connected to the second IF output terminal 134, a third LO transistor 123 which has a source terminal connected to the drain terminal of the second RF transistor 112 and a drain terminal connected to the ~~third~~ first IF output terminal 133, and a fourth LO transistor 124 which has a source terminal connected to the drain terminal of the second RF transistor 112 and a drain terminal connected to the ~~fourth~~ second IF output terminal 134.

wf 7-20-09 4) On page 53, lines ~~13~~ 2 and 15, please amend the following paragraph as follows:

As shown in Fig.14, the mixer circuit according to the ~~*third*~~ sixth embodiment includes, in addition to that the fifth embodiment of the resent invention is provided with the first and second ~~bias~~ bypass current sources 145 and 146 that additionally supply the bias currents only to the first and second RF transistors 111 and 112, further a third bypass current source 147 that is connected between the first IF output terminal 133 and the ground GND thereby to additionally supply a bias current only to the first load resistor 131, and a fourth bypass current source 148 which is connected between the second IF output terminal 134 and the ground GND thereby to additionally supply a bias current only to the second load resistor 132. These first to fourth bypass current sources 145 to 148 are covered in a bypass current supply portion described in Claim 13.